
Chapter 8 — PRI Maintenance

Overview

This chapter provides an overview of the maintenance tools available for 2.0 Mb PRI or ISL features:

- commands used to maintain PRI, DDCH, DCHI and clock controller hardware
- tests for 2 Mb PRI operation
- error detection for 2 Mb PRI, including the various thresholds found in the 2 Mb PRI loop timers in LD 73.

Enabling the 2 Mb PRI after installation

To enable an NTAK79 or NTBK50 PRI circuit pack, follow the appropriate procedure below.

Enabling the NTAK79 PRI

- 1 Software enable all 2 Mb PRI cards using overlay 60 (command ENLL N). The DCHI will enable automatically from the enable PRI command.
- 2 Software enable the clock controller using overlay 60 (command ENL CC 0).
- 3 Enable clock tracking on primary digital loop by issuing the following command: TRCK PCK.

Within about 30 seconds the D-channel layer 3 should be established.

- 4 You can request the current status of the D-channel by issuing the command STAT DCH. The system should respond DCH N EST in LD 96 (meaning that the D-channel is established and operational).

Enabling the NTB50 PRI

- 1 If using the NTB51 DDCH daughterboard, enable the DDCH in LD 96 by issuing the command ENL MSDL X.
- 2 Software enable all 2 Mb PRI cards using overlay 60 (command ENLL N). The DCHI will enable automatically from the enable PRI command.
- 3 Software enable the clock controller using overlay 60 (command ENL CC 0).
- 4 Enable clock tracking on primary digital loop by issuing the following command: TRCK PCK.

Within about 30 seconds the D-channel layer 3 should be established.

- 5 You can request the current status of the D-channel by issuing the command STAT DCH. The system should respond DCH N EST in LD 96 (meaning that the D-channel is established and operational).

Disabling the 2 Mb PRI before removal

To disable a PRI circuit pack, follow the appropriate procedure below.

Disabling the NTAK79 PRI

- 1 Software disable the DCHI using overlay 96, command DIS DCH N, where N is the D-channel device number.
- 2 Software disable the clock controller using overlay 60 (DIS CC 0).
- 3 Software disable the PRI card using overlay 60 (command DISL N, where N is the PRI card number).

Disabling the NTB50 PRI

- 1 Software disable the DCHI using overlay 96, command DIS DCH N, where N is the D-channel device number.
- 2 If using the NTB51 DDCH daughterboard, enter the DIS MSDL N command in overlay 96.
- 3 Software disable the clock controller using overlay 60 (DIS CC 0).

- 4 Software disable the PRI card using overlay 60 (command DISL N, where N is the PRI card number).

Monitoring Option 11 PRI operation

Maintenance messages

Service messages report on near and far end switch status. Both service and service acknowledge messages are supported on PRI B-channels and ISL channels. These messages are used for backup D channel and D channel sanity polling. The status may be in-service and out-of-service.

Service and service acknowledge messages for B-channels and ISL channels are supported between:

- Meridian 1 to Meridian 1: ISL and PRI
- Meridian 1 to CO: PRI only

The status of these messages is reported by the service and service acknowledge messages for B-channels and ISL channels:

- in-service
- maintenance
- out-of-service

Near end and far end subcategories are defined for each maintenance status. See Table 32 for possible combinations of near end and far end status, and the channel capability for each status. When the status of the near end and far end does not match, the more severe maintenance status takes effect over the less severe maintenance status.

Table 32
Maintenance message status

Near end status	Far end status	B channel capability
In-service	In-service	both incoming and outgoing calls allowed
In-service	Maintenance	only incoming calls allowed
In-service	Out-of-service	not allowed to use
Maintenance	N/A	not allowed to use
Out-of-service	N/A	not allowed to use

Service message function

Service messages are used to monitor the following:

- D-channel establishment
- D-channel sanity polling
- B-channel or ISL status change
- Channel status audit.

D-channel establishment

When the D-channel establishes, the B-channel status is supported by sending service messages for each B-channel controlled by a D-channel. This allows the far end to synchronize its channel states. These services messages are sent when the D-channel is brought up automatically by the system or manually by using LD 96.

D-channel sanity polling

If a D-channel has been idle for 30 seconds, a service message is sent to poll the sanity of the link. The service message is sent regardless of whether the near end is configured as master or slave.

B-channel status change

Whenever there is a status change for a B-channel or an ISL channel, the new status is reported to the far end in a service message. Status change can occur through service change or maintenance operations, such as the addition or deletion of a channel in LD 14, or disabling of the associated loop, shelf, card or unit in LD 30, LD 32, LD 36, LD 41 or LD 60.

Channel status audit

LD 30 is enhanced to allow channel status audit to be initiated. The channels associated with each D-channel are examined and their status is reported to the far end by service messages.

Service message commands

You activate the service messages in LD 96 on a per D-channel basis. The commands are:

- ENL SERV N: turns on the support of service and service acknowledge messages for DCH link N. The command should only be executed when the specified D-channel is in the disabled state.

- DIS SERV N: turns off the support of service and service acknowledge messages for DCH link N.
- STAT SERV (N): displays the current service and service acknowledge message SERV setting for individual DDCH N or for DCHIs.

When configuring these messages, the SERV command should only be enabled if both switches are equipped with a minimum of X11 release 15 software.

Two new statuses are added for maintenance messages, FE MbSY = Far end maintenance and FE DSBL = Far end disabled.

2 Mb PRI error detection

The Primary Rate Interface categorizes errors and alarm conditions into two main groups, Group I and Group II errors.

Group I Errors

These are real-time calculated error-rate thresholds. Group I errors can include:

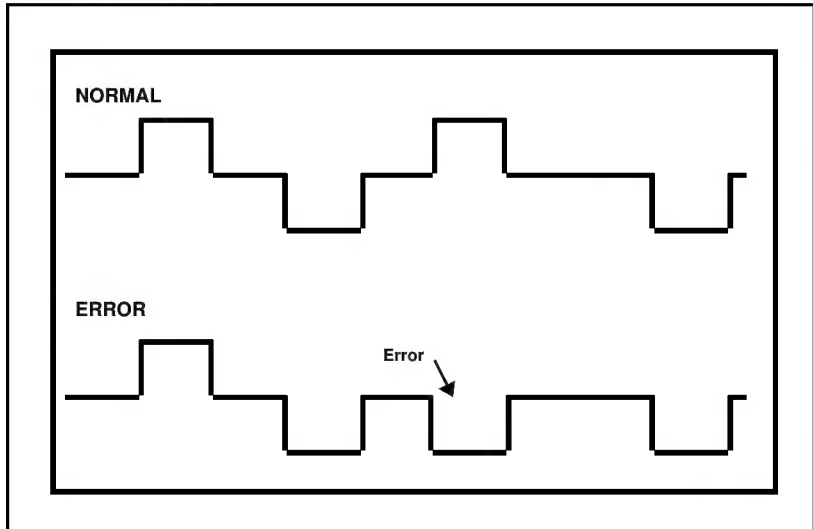
- Bipolar Violations (BPV)
- Frame Bit Errors (FBER)
- CRC-4 Word Errors (CRC)
- Controlled Frame Slips

Bipolar Violations

In a alternate mark inversion (AMI) bipolar pulse stream, pulses alternate in polarity. A bipolar violation has occurred when two pulses of the same polarity are received in succession, as shown in Figure 77. This might be caused by an electrical disturbance such as noise, a low signal level or a faulty repeater. Bipolar violations give a good indication of the integrity of the local span from the Meridian 1 to the first repeater.

The PRI card, following the CEPT PCM-30, uses a zero code suppression technique known as HDB3 which introduces intentional bipolar violations onto the carrier. This is accounted for by the receiver and disregarded as bipolar violation errors.

Figure 77
Bipolar violations



Frame Bit Errors

The NTAK79/NTBK50 PRI CEPT PCM-30 stream is structured into a frame of 32 8-bit timeslots. To maintain alignment of this frame structure, alternate timeslot zeros have a specific frame alignment pattern (X0011011).

A frame bit error is acknowledged when any of the bits in the received pattern are in error. This error rate provides an indication of the integrity of the complete end-to-end span.

CRC-4 Word Errors

When operating in the CRC-4 multiframe format (CRC), frames are bundled into groups of 16. This format includes a specific multiframe alignment pattern in bit 0 of every even frame's timeslot 0 (001011XX).

Each odd frame timeslot 0 includes a CRC-4 cyclic redundancy checksum of the previous 8 frames (sub-multiframe). This transmitted checksum is compared against a calculated checksum at the receiver. If the two checksums do not match, a CRC-4 Word error is indicated.

Group I error rates are processed on the PRI card based on software downloadable parameters N1 and N2 (for each BPV, CRC and FBER). The values for N1 are scaled on the card as follows:

— $BPV = N1 \cdot 16$

— $CRC = N1 \cdot 4$

— $FBER = N1 \cdot 1$

N2 values are not scaled. These parameters may be established in LD 73 on a per card basis, or they can be left at their default values.

Parameters N1 and N2 provide for the following error rate thresholds reported to the system:

Severely Errored Second: when the number of occurrences of the error exceeds the value of N1 in the previous second. This error is reported and counted (LCNT), but no action is taken by the system.

Unavailable Condition: this is reported when 10 severely errored seconds are received in 10 consecutive seconds. This is equivalent to an error rate worse than 10^{-3} with the default value. When this condition is reached, the 2 Mb PRI is put into an out-of-service condition until the Group I OOS guard timer expires and the error condition has ceased or improved.

No New Call Condition: when the number of occurrences of the error exceeds the value of $(10 \times N2)$ in the previous minute. This corresponds to an error rate of 10^{-3} to 10^{-5} using the default N2 value. When this condition is reported, the system will record the error (LCNT) and place the PRI card into a no new call condition, with all idle channels set to MbSY. The card automatically returns to normal state when the condition improves after the Group I NNC guard timer expires.

Maintenance Condition: this condition implements when the number of occurrences of the error exceeds the value of N2 in the previous minute. This corresponds to an error rate between 10^{-5} and 10^{-6} based on the N2 default values. When this condition is reported, the system will record the error (LCNT) and place the 2 Mb PRI card into a maintenance alarm state. This state has no effect on call processing but simply alerts you of the line degradation. The card automatically returns to normal state when the condition improves after the Group I MAINT guard timer expires.

There is no error report for the error rates below 10^{-6} (10xN2), as such rates are considered satisfactory.

Programming Group I Thresholds

To set your Group I thresholds, use the following commands in LD 73:

Prompt	Response	Description
REQ	CHG	
TYPE	PRI2	
FEAT	LPT1	
•		
BPV	N1 N2	default: 128 122
CRC	N1 N2	default: 201 97
FBER	N1 N2	default: 28 1
•		
OOS1	1 - 60 M	default: 15
NNC1	1 - 60 M	default: 15
MNT1	1 - 60 M	default: 15

Frame Slips

Digital signals must have accurate clock synchronization for data to be interleaved into or extracted from the appropriate timeslot during multiplexing and demultiplexing operations. A Frame Slip is defined (for 2 Mb links) as the repetition of, or deletion of the 256 data bits of a CEPT frame due to a sufficiently large discrepancy in the read and write rates at the buffer (clocks aren't operating at EXACTLY the same speed).

When data bits are written into (added to) a buffer at a slightly *higher* rate than that at which they are being read (emptied), sooner or later the buffer overflows. This is a slip-frame deletion.

In the opposite situation, when data bits are written (added) into a buffer at slightly *lower* rate than that at which they are being read (emptied), eventually the buffer runs dry or underflows. This is also a slip-frame repetition.

A 2 Mb PRI contains a buffer large enough to contain 2 full frames ($256 \times 2 = 512$ bits), and is normally kept half full (1 frame). See the following table for the impact of one slip on various types of data.

All of the degradations shown in the following table can be controlled or avoided by proper clock (network) synchronization.

Performance Impact of one Slip.

Service	Potential Impact
Encrypted Text	Encryption key must be resent.
Video	Freeze frame for several seconds. Loud pop on audio.
Digital Data	Deletion or repetition of Data. Possible Misframe.
Facsimile	Deletion of 4-8 scan lines. Drop Call.
Voice Band Data	Transmission Errors for 0.01 to 2 s. Drop Call.
Voice	Possible Click

Clock synchronization can be either tracking, on the primary or secondary reference clock, or free run (non-tracking). In LD 73 (prompts PREF and SREF), the 2 Mb PRI which supports the clock controller is defined as the primary clock reference. Another 2 Mb PRI (or DTI) may be defined as the secondary clock reference. The clock controller synchronizes from the primary or secondary's references incoming bit stream. The clock controller in turn supplies a synchronized reference for the rest of the system, including all 2 Mb PRIs and DTIs.

The 2.0 Mb PRI card detects and reports frame slips (repetitions and deletions) to the Meridian 1. The count of slips is recorded (LCNT), printed out, and cleared at each midnight routine.

Frame slips have two alarm thresholds as defined in LD 73. They are as follows:

Slip - Out of Service Threshold

When this threshold (variable count versus variable time) is reached, the PRI card is placed in an out-of-service state. The card automatically returns to a normal state if the slip rate improves after the Group I OOS guard timer expires.

Slip - Maintenance Threshold

When this threshold is reached, the PRI card is placed in an maintenance state that has no impact on call processing. The maintenance state is simply an indication that a degraded condition exists. The card automatically returns to a normal state if the slip rate improves after the Group I MAINT guard timer expires.

Defining Slip Thresholds

To define your slip thresholds, use the following commands in LD 73:

Prompt	Response	Description
REQ	CHG	
TYPE	PRI2	
FEAT	LPTI	
•		
SLIP	5 24H (This entry establishes a maintenance threshold of 5 slips in 24 hours)	20 1H (This entry establishes an OOS threshold of 20H [32] slips in 1 hour)

Times range from 1M to 24H (1 minute to 24 hours). Counts are 1 to 255.

Group II Errors

Group II errors are event-based alarms that can be separated into Red (local) and Yellow (far end) alarms.

Yellow (Far End) Alarms

A Yellow alarm on the 2.0 Mb PRI card indicates that the card is receiving an alarm indication from the far end.

This type of alarm may be received in two ways:

- **Remote Alarm Indication (RAI)**—Bit 3 of non-FAS frame set
or,
- **Alarm Indication Signal (AIS)**—All 1s on the carrier.

Since the 2 Mb PRI is receiving a Yellow alarm signal, that indicates that there is a carrier connection, but the far end is not ready. It is possible, however, that the carrier connection is one way only (2 Mb PRI receiving).

When the 2 Mb PRI receives a Yellow alarm signal, all channels are placed in a maintenance busy mode (MBSY). Group II Yellow alarms are recorded (LCNT) on each occurrence, but the card is not placed into an out-of-service state.

Red (Local) Alarms

A Red alarm on the PRI card indicates that the card is having problems synchronizing with the incoming bit stream.

This type of alarm may be caused by the following:

- **Loss of Signal (LOS)**
- **Loss of Frame Alignment (LFAS)**
- **Loss of CRC-4 Multiframe Alignment (LMAS)**

When the 2 Mb PRI is in a Red alarm state, RAI is transmitted to the far end.

For both Group II Red and Yellow alarm states, action is taken after the condition has persisted for a downloaded persistence (PERS) threshold. The parameter is set in LD 73 in multiples of 2 msec, with $2 \times 50 = 100$ msec as the default.

For Group II Red alarm conditions, there are four definable time thresholds that can be set in LD 73 on a per-loop basis. The first parameter sets an aggregate time in multiples of 128 msec (default $20 \times 128 = 2.5$ sec). The next four parameters provide time thresholds for MAINT, NNDC, NNC and OOS.

For example, if the total cumulative time that an error has been present reaches the aggregate time (2.5 sec default) in less than the time set in OOS, the card is put into an out-of-service state. If it took more than the preset time for the error condition to register, the card could be put into NNDC, NNC or MAINT states. The card remains in the alarm condition until the error has improves and after the Group II guard timers expire.

Defining Group II Error Thresholds

You are able to define Group II error thresholds in LD 73, as follows:

Prompt	Response	Description			
TYPE	2 Mb PRI				
FEAT	LPTI				
.					
GP2	20 (Aggregate count default [20x128ms= 2.5sec])	100s (Maintenance threshold)	12s (NNDC threshold)	12s (NNC threshold)	4s (OOS threshold)
.					
OOS2	1-(15)-255s	(Group II guard timer)			
NNC2	1-(15)-255s	(Group II guard timer)			
MNT2	1-(15)-255s	(Group II guard timer)			
PERS	50	(in multiples of 2ms)			
CLRS	50	(in multiples of 2ms)			
OOSC	1-(5)-255	(Out of service count limit) After this number is reached, the card does not auto-enable.			

Only the highest priority Group II alarm condition is active at a time. The order of priority (from highest to lowest) is: LOS, AIS, LFAS, LMAS, RAI.

NTAK79 Faceplate LEDs

The NTA79 circuit card has a total of seven faceplate LEDs. Five of the LEDs are directly associated with the operation of the Primary Rate interface (PRI). The remaining two LEDs are associated with the on-board Clock Controller and the on-board D-channel interface (DCHI).

NTAK79 faceplate LEDs

LED	State	Definition
OOS	On (Red)	The NTA79 2 Mb PRI circuit card is either disabled or out-of-service.
	Off	The NTA79 2 Mb PRI is not in a disabled state.
ACT	On (Green)	The NTA79 2 Mb PRI circuit card is in an active state.
	Off	The NTA79 2 Mb PRI is in a disabled state. The OOS LED is red.
RED	On (Red)	A red alarm state has been detected. This represents a local alarm state of Loss of Carrier (LOS), Loss of Frame (LFAS) or Loss of CRC Multiframe (LMAS).
	Off	No red (local) alarm.
YEL	On (Yellow)	A yellow alarm state has been detected. This represents a remote alarm indication from the far end. The alarm may be either Alarm Indication (AIS) or Remote Alarm (RAI).
	Off	No yellow (remote) alarm.
LBK	On (Green)	NTA79 2 Mb PRI is in loop-back mode.
	Off	NTA79 2 Mb PRI is not in loop-back mode

NTAK79 faceplate LEDs (continued)

LED	State	Definition
CC	On (Red)	The clock controller is switched on and software disabled
	On (Green)	The clock controller is enabled and is either locked to a reference or is in free run mode
	Flashing (Green)	The clock controller is enabled and is locking onto a reference.
	Off	The clock controller is switched off (by switch SW3).
DCH	On (Red)	DCHI is switched on and disabled
	On (Green)	DCHI is switched on and enabled, but not necessarily established.
	Off	DCHI is switched off (by switch SW1).

NTBK50 Faceplate LEDs

The NTBK50 circuit card has a total of seven faceplate LEDs. Five of the LEDs are directly associated with the operation of the Downloadable D-Channel handler and D-Channel interface. The remaining two LEDs are associated with the Clock Controller.

NTBK50 faceplate LEDs

LED	State	Definition
OOS	On (Red)	The NTBK50 2 Mb PRI circuit card is either disabled or out-of-service. Also, the state of the card after power-up, completion of self test, and exiting remote loopback.
	Off	NTBK50 is not in a disabled state.
ACT	On (Green)	NTBK50 PRI circuit card is in an active state.
	Off	NTBK50 2 Mb PRI is in a disabled state. The OOS LED is red.
RED	On (Red)	A red alarm state has been detected. This represents a local alarm state of Loss of Carrier (LOS), Loss of Frame (LFAS) or Loss of CRC Multiframe (LMAS).
	Off	No red (local) alarm.
YEL	On (Yellow)	A yellow alarm state has been detected. This represents a remote alarm indication from the far end. The alarm may be either Alarm Indication (AIS) or Remote Alarm (RAI).
	Off	No yellow (remote) alarm.
LBK	On (Green)	NTBK50 2 Mb PRI is in loop-back mode.
	Off	NTBK50 2 Mb PRI is not in loop-back mode

NTBK50 faceplate LEDs (continued)

LED	State	Definition
CC	On (Red)	The clock controller is software disabled
	On (Green)	The clock controller is enabled and is either locked to a reference or is in free run mode
	Flashing (Green)	NTAK20 is equipped and is attempting to lock (tracking mode) to a reference. If the LED flashes continuously over an extended period of time, check the CC STAT in LD60. If the CC is tracking this may be an acceptable state. Check for slips and related clock controller error conditions. If none exist, then this state is acceptable, and the flashing is identifying jitter on the reference.
	Off	The clock controller is not equipped.
DCH	On (Red)	DCH is disabled.
	On (Green)	DCH is enabled, but not necessarily established.
	Off	DCH is not equipped.

Using Option 11 PRI maintenance tools

2 Mb PRI commands (LD 60)

Command	Action
DISI L	disable 2 Mb PRI when idle
DISL L	force disable PRI
ENLL L	enable PRI
LCNT (L)	list alarm counters
RCNT (L)	reset alarm counters and clear alarms
SLFT (L)	do 2 Mb PRI self-test (2 Mb PRI must be disabled first)
STAT (L)	list 2 Mb PRI status
RLBK L (C)	enable remote loopback
DLBK L (C)	disable remote loopback
RMST L (C)	Perform remote loopback

PRI status and error conditions are reported in the following types of messages. These messages can be found in the X11 Software Guide - Including Supplementary Features.

DCHI commands

D-channel commands are found in LD 96. The following is a quick reference list of D-channel commands:

Command	Action
DIS DCHI N	disable DCHI port N
ENL DCHI N	enable DCHI port N
EST DCH N	establish D-channel N
PLOG DCHI N	print D-channel statistics log N
RLS DCH N	release D-channel N
SDCH DCH N	release a D-channel and switch D-channels
RST DCH N	reset D-channel N
STAT DCH (N)	print D-channel status (link status)
TEST 100/101	DCH tests
STAT SERV	Print the current service and service acknowledge message for DCHI N
ENL SERV N	enable service messages for DCHI N
DIS SERV N	disable service messages for DCHI N

D-channel status and error conditions are reported as DCH messages. These messages can be found in the Option 11 *Software guide*.

DDCH commands

Downloadable D-channel commands are found in LD 96. The following is a quick reference list of D-channel commands with minor modification:

Command	Action
DIS MSDL X (ALL)	disable DCHI card X
ENL MSDL X (FDL, ALL)	enable DCHI card X, with or without Force Download
RST MSDL X	Reset MSDL card X
STAT MSDL X (X (full))	Get MSDL status X, or a "FULL STATUS"
SLFT MSDL X	Execute a self test on MSDL card X
DIS LLB X	Disable local loop back on MSDL DCH X
DIS RLB X	Disable remote loop back on MSDL DCH X
DIS TEST X	Disable Test mode on MSDL DCH X
ENL LLB X	Enable local loop on MSDL DCH X
ENL RLB X	Enable remote loop on MSDL DCH X
ENL TEST X	Enable Test mode on MSDL DCH X
PCON DCH X	Print configuration parameters on MSDL DCH X
PMES DCH X	Print incoming layer 3 messages on MSDL DCH X
PTRF DCH X	Print traffic report on MSDL DCHX
TEST LLB X	Start local loop back test on MSDL DCH X
TEST RLB X	Start remote loop back test on MSDL DCH X

Note: "X" represents the D-Channel device number

D-channel status and error conditions are reported as DCH messages. These messages can be found in the Input/Output guide.

Clock Controller commands

Clock Controller commands are accessed using LD 60. The following is a quick reference list of clock controller commands:

Command	Action
DIS CC 0	disable clock controller
ENL CC 0	enable clock controller
SSCK 0	status of clock controller
TRCK XXX	set clock controller tracking where XXX can be: PCK—track primary clock reference source SCLK—track secondary clock reference source FRUN—free run mode

NTAK79/NTBK50 Power on self test

When power is applied to the NTAK79/NTBK50 2 Mb PRI circuit card, the card performs a power-on self-test. The self-tests verify the operation of most of the on-board hardware.

If all the self-tests pass, the upper 5 LEDs blink simultaneously three times. If any of the self-tests fail, the LEDs do not blink. Only the OOS LED illuminates. The corresponding error code is then printed on the TTY.

Self-test error codes

The following table lists the self test failure codes for the NTAK79/NTBK50 2 Mb PRI. These codes could be returned on card power-up in the form “DTA105 L X” (where X is the failure code), or during a self test procedure in LD 60 as “DTI009 L X” (where X is the error code).

Failure codes 1-14 are hardware failures on the NTAK79/NTBK50 card. Codes 15-16 may be due to carrier span problems or lack of loopback activation at the far end.

Failure Code	Associated Error
0	Self test passed
1	Self test general failure
2	LCAs failed to program correctly
3	8031 code checksum failure
4	8031 internal RAM failure
5	8031 external RAM failure
6	PAD RAM failure
7	AO7 signaling interface failure
8	UART (card LAN) failure
9	CEPT transceiver failure
10	Line interface failure
11	Receiver framing failure
12	Transmit/receive (inter)national bit failure
13	Yellow (remote) alarm failure
14	PCM path integrity failure
15	Loop remote loopback failure
16	Channel remote loopback failure

2 Mb PRI self test

This self test can be run manually on a per-loop or per channel basis using overlay 60. The DCHI/DDCH and 2 Mb PRI must be disabled before performing the self-test.

Self-test (entire loop)

- 1 Disable the DCHI/DDCH using:

LD 96

DIS DCH N

- 2 Disable the 2 Mb PRI card and run the self-test using:

LD 60

DISL L

SLFT L (entire loop)

Self-test (specific channel)

DSCH L CH (disable an idle channel)

SLFT L CH (specific channel)

2 Mb PRI automatic loop test

This procedure is not recommended since it causes yellow at the far-end and there is a possibility of some of the B-channels not being re-enabled once the test is completed. Therefore leave the ATLP command set to 0.

The automatic loop test checks the same functions as the self test. Unlike the self test, it can be run automatically as part of the midnight routines.

Procedure (2 Mb PRI automatic loop test):

- 1 With ATLP command set to one.
- 2 If all 30 channels are idle at midnight, the Meridian 1 software disables the card and performs a self test on all channels. This causes a yellow alarm to be generated to the far end.

- 3 If any of the 30 channels are busy at midnight, the software disables one idle channel, chosen at random, and checks it while the card is enabled.

With the ATLP command set to zero, only one channel is tested. The channel tested is randomly selected by software; it cannot be specified.

To perform the automatic loop test as part of midnight routines, use

LD 60

ATLP 1 or 0

Link diagnostic and remote loop back tests

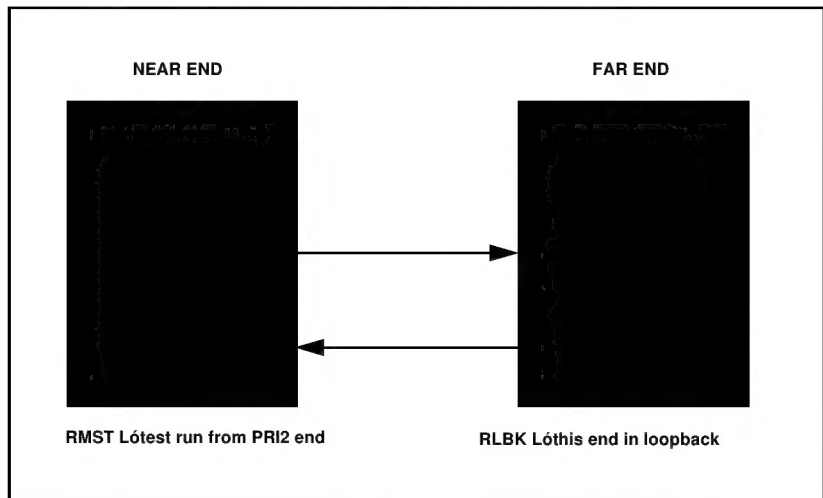
The remote loop-back and the link diagnostic test are performed manually on a per channel or per-loop (or card) basis.

Link diagnostic test

The link diagnostic test, also called the far end loop-back test, does not test the Meridian 1 2 Mb PRI. It puts the 2 Mb PRI in loop-back mode so a remote loop-back test can be performed on equipment at the far end. (See Figure 78.)

The 2 Mb PRI channel or loop (card) tested must be disabled.

Figure 78
2 Mb PRI Link Diagnostic (Far End Loopback) Test



Running the link diagnostic test

To run the link diagnostic test on the Meridian 1, use the following procedure:

- 1** Call a technician at the far end. Ask for loopback mode at that facility.
- 2** When loop-back mode at the far end is confirmed:

- Disable the DCHI/DDCH using:

LD 96

DIS DCH N

- Disable the 2 Mb PRI card and run loop-back test using:

LD 60

DISL L

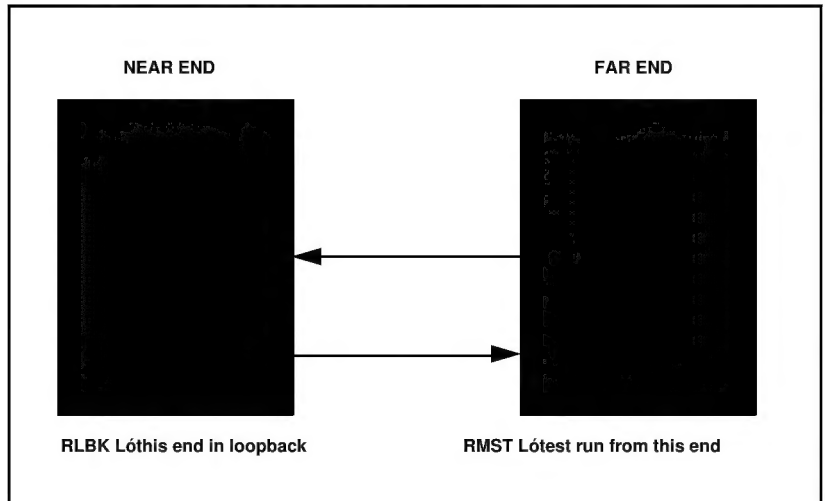
RMST L or RMST L C

Remote loop-back test

The remote loop-back test also called the near end loop-back test, checks the integrity of the 2 Mb PRI from the Meridian 1 system to the far end. The far end must be in loop-back mode before this test can be performed. (See Figure 79.)

The 2 Mb PRI channel or loop (card) tested must be disabled.

Figure 79
2 Mb PRI Remote Loopback Test



Coordinating the remote loopback tests

When a technician at the far end asks for loop-back mode on the Meridian 1:

Disable the DCHI/DDCH using:

LD 96

DIS DCH N

Disable the 2 Mb PRI card and activate loopback mode using:

LD 60

DISL L

RLBK L or RLBK L C